REMARKS

Claims 1-16 are presently pending in the application.

The Office Action rejected claims 1-16 on prior art. Regarding these rejections, claims 1-3, 5-7, 10, 15 and 16 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keller et al. (U.S. Patent No. 5,985,719) in view of Wada et al. (U.S. Patent No. 5,087,584); claim 4 was rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keller et al. in view of Wada et al. as applied to claims 1-3, 5-7, 10, 15 and 16, and further in view of Kokubu (U.S. Patent No. 6,200,858); claims 8-9 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keller et al. in view of Wada et al. as applied to claims 1-3, 5-7, 10, 15 and 16, and further in view of view of Tay et al. (U.S. Publication No. US2002/0009900); claims 11-12 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keller et al. in view of Wada et al. and further in Tay et al. as applied to claims 8-9, and further in view of view of Ma et al. (U.S. Patent No. 6,207,586); and claims 13 and 14 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Keller et al. in view of Wada et al. as applied to claims 1-3, 5-7, 10, 15 and 16, and further in view of Gill (U.S. Patent No. 5,420,060). Applicants respectfully traverse these rejections.

In accordance with an aspect of the present invention, a SiN barrier layer can be added onto a flash memory word-line sidewall to attenuate or prevent the so called "over-erase" issue. For flash memory structures such as described in Applicants' specification, higher electrical fields tend to exist at the four corners of a memory-cell channel during Fowler-Nordheim (F-N) erase operations. Thus, such operations tend to cause over-erase phenomena by way of electrons being more apt to tunnel out through these four corners. By adding a SiN barrier layer along the sidewall of the word line, the tunneling electrons at the mentioned corners can be captured by the SiN barrier layer, and the edge electrical field can be reduced to thereby effectively close the relatively easy tunneling paths. Thus, in accordance with an aspect of the present invention, a SiN barrier layer can be added on the word-line sidewall for enhanced operation of the resulting memory device. Furthermore,

regarding the oxide layer, which is deposited before the SiN barrier layer, this oxide layer can in the context of the presently claimed invention improve flash memory reliability, since, for example, the SiN barrier layer material can undergo higher mechanical stress and the tunneling oxide can be damaged after SiN deposition and following thermal processes. This oxide layer can thus act as a stress release layer for the SiN barrier layer.

In connection with the various prior-art rejections of the current claims, these prior art references, when considered alone or in combination, do not appear to teach or suggest, for example, Applicants' claimed liner dielectric layer and barrier layer together extending in a direction transverse to the bit line direction and substantially parallel to the control gate, as recited, for example, in independent, amended claim 1.

Regarding this exemplary limitation (of the liner and barrier layer orientations), the Examiner in the outstanding Office Action correctly acknowledged that Keller et al. is devoid of any express disclosure of the liner direction extending in a direction transverse to a bit line.

Following this acknowledgment, however, the Office Action concluded, without citing to additional references or providing adequate reasoning as to the relevance of Wada et al. and its suitability for being combined with Keller et al., that "it would have been obvious ... to modify the process of Keller et al. so as to form the liner transverse to the bitline [sic] ...."

1. None of the Prior-Art References of Record Disclose Liner/Barrier Layers Extending in the Word-Line Direction.

It is well established that a claim can be rejected on obviousness grounds only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior-art reference or combination of prior-art references. Thus, for a rejection under 35 U.S.C. 103(a) to be proper, every limitation recited in a rejected claim must be disclosed or taught somewhere in the collection of prior-art references. In the instant case,

Applicants respectfully submit that the cited references neither disclose nor suggest each and every element that is recited in the rejected claims. Accordingly, as set forth below, the outstanding rejections under 35 U.S.C. § 103(a) are improper and should be withdrawn.

In the instant case, applying the above standard, the prior art references of record, taken separately or together, neither disclose, teach nor suggest any of Applicants' claimed combinations of processes for forming memory devices, including, among other things, "providing a stacked structure ... comprising a first dielectric, a floating gate, a second dielectric, and a control gate; forming a liner dielectric layer, which extends in a direction transverse to a bit line direction and substantially parallel to the control gate, on sidewalls of the stacked structure; and forming a barrier layer on at least part of the liner dielectric layer" (emphasis added), as recited in independent, amended claim 1.

2. No Plausible Motivation Has Been Provided to Combine the Keller et al. and Wada et al. References for a Proper Rejection of Claim 1.

After noting the deficiency of Keller et al., the Office Action then looked to the disclosure of Wada et al. for a purported teaching that "it is conventional memory architecture to have the floating and control gate stack transverse to the bit [sic] line." Applicant submits that such an alleged teaching, even if hypothetically assumed, arguendo, to be correct, does not in any way provide support for the present obviousness rejection of the current claims. A person of ordinary skill in the art at the time of the invention, having possession of the disclosure of Keller et al. and the above-alleged teaching of Wada et al., would not even think to combine the two references and, certainly, would not have been motivated to do so. The mere fact that floating and control gate stacks can be formed transverse to bit lines would not lead one of ordinary skill in the art to combine Wada et al. with Keller et al. It is submitted, for example, that a skilled artesian would not seek to combine the teachings of (1) Keller et al. and his shield layer 44 that would appear to be used for a barrier characteristics capability for moisture and sodium as discussed in col. 4, lines 57-67, with the teachings of (2) Wada et al. and his quite divergent apparent focus on contactless formation methods. (To the extent that Wada et al. is relied upon only to show

the formation of such stacks in word-line directions, it is submitted that a combination of this concept with Keller et al. would not yield the limitations of Applicants' claimed invention, as discussed below.)

3. A Combination of Keller et al. and Wada et al., Even if Contrived, Still Would Not Yield Applicants' the Invention of Claim 1.

The purported teaching of Wada et al. "to have the floating and control gate stack transverse to the bit [sic] line," if combined with the disclosure of Kelly et al., would not teach or suggest Applicants' claimed invention. A person of ordinary skill in the art at the time of the invention, having knowledge of the alleged teaching of Wada et al. and the disclosure of Keller et al, would not have thought to combine the two references to yield Applicants' claimed invention and, certainly, would not have been motivated to do so. For instance, a skilled artesian following the alleged disclosure of Keller et al. to place liners in directions parallel to bit lines, would not, upon a reading of Wada et al. and its alleged teaching to form "the floating and control gate stack transverse to the bit [sic] line," be motivated to change the direction of the liner and barrier layers in order to meet Applicants claimed processes that provide liner and barrier layers for capturing electrons at the four corners of memory channels during F-N erase operations. In fact, a skilled artesian could just as well, to the extent he or she hypothetically could or would make any combination of these two references, have placed liners in directions parallel to bit lines in the structure of Wada et al. Indeed, to the extent the two references could or would even be combined at all (e.g., the shield layer 44 of Keller et al. is used for its barrier characteristics capability for moisture and sodium as discussed in col. 4, lines 57-67, and the focus of Wada et al. is on contactless formation methods), the cumulative teachings of these references are still devoid of any orientation of a liner dielectric layer and a barrier layer to extend in a direction transverse to the bit line and substantially parallel to the control gate.

4. Allowable Subject Matter is Further Defined in Dependent Claims, Such as Claims 15 and 16.

The Office Action addressed the limitations of several of the dependent claims, including claims 15 and 16, by simply pointing to a disclosure in a prior art reference that purportedly shows that limitation. In other words, the Office Action did not provide, in Applicants' opinion, adequate reasoning as to why one of ordinary skill in the art would have been motivated to combine certain references to yield processes that meet all of the limitations of each dependent claim and the base claim(s) from which it depends. Applicants respectfully submit that each of the dependent claims, such as claims 15 and 16, is allowable at least because of its incorporation by reference of the allowable subject matter from the respective independent claim 1, and further because of the additional limitations recited in the dependent claim. With regard to claims 15 and 16, for example, the Office Action rejected these claims with a statement to the effect of: "note that the liner dielectric 42 and the barrier layer 44 in Keller et al. are formed to extend over some source/drain regions and not to extend over other source/drain regions (see fig.7)." As described above, however, even if the Examiner's noting of the locations of layers 42 and 44 of Keller et al. were correct, such a hypothetical combination with Wada et al. would only yield, in a best case scenario according to Applicants' opinion, the layers 42 and 44 on a structure of Wada et al. extending in directions parallel to bit lines rather than word lines.

As discussed, it is submitted that the presently pending dependent claims are allowable at least because of their dependencies upon independent, amended claim 1, and further because of the additional limitations recited in those dependent claims.

Applicants respectfully request reconsideration and withdrawal of the rejections of the presently pending claims under 35 U.S.C. §103(a).

In view of the above, it is respectfully submitted that the application is now in condition for allowance, and an early indication of same is requested. The Examiner is invited to contact the undersigned with any questions.

Respectfully submitted,

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